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(54) **OLED DISPLAY PANEL AND OLED DISPLAY DEVICE COMPRISING THE SAME**

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(57) **ABSTRACT**

The present disclosure relates to an OLED display panel for minimizing the size of a bezel and includes: an active area including data lines, scan lines intersecting the data lines, and sub-pixels arranged at each intersection; and a stage of a GIP driving circuit distributed and arranged in a plurality of unit pixel regions driven by m (m being a natural number) scan lines in the active area, to supply scan pulses to the corresponding scan lines, wherein the active area further includes m GIP internal connection lines parts respectively adjacent to the m scan lines, and a plurality of internal connection lines for connecting elements constituting each stage is distributed and arranged in the m GIP internal connection line parts.

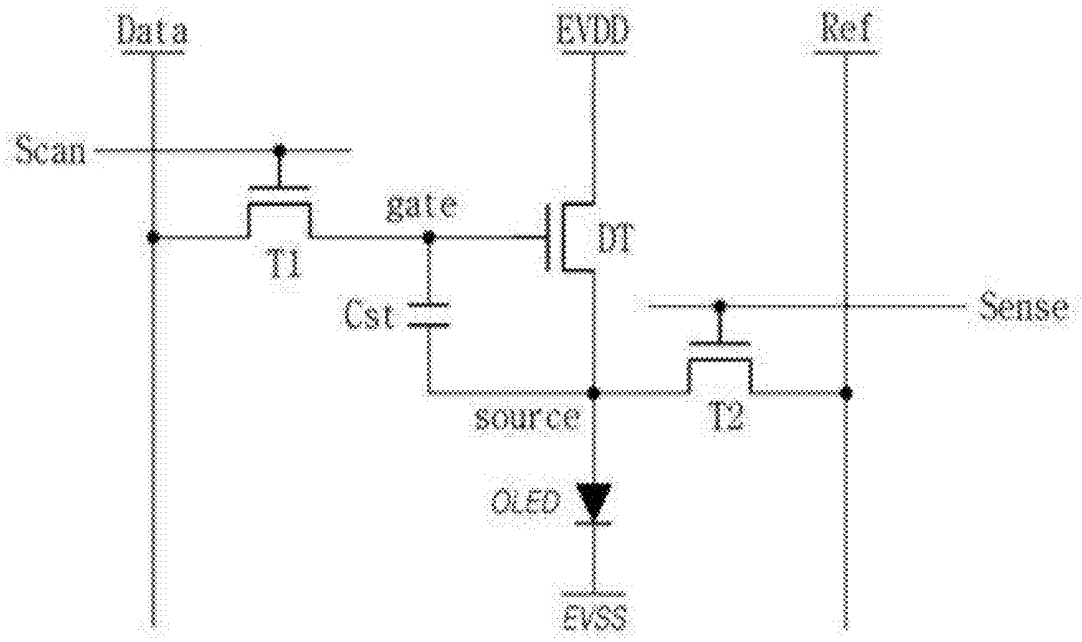


FIG. 1

Related Art

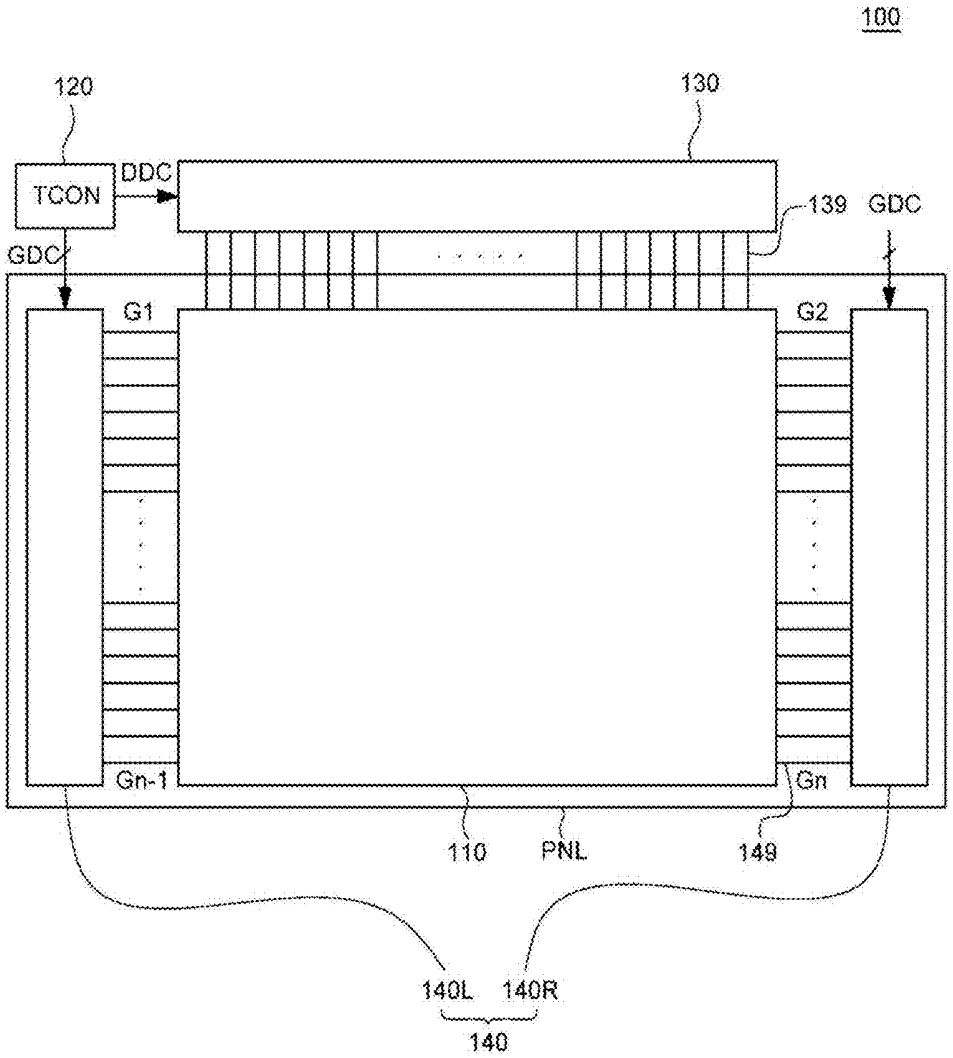


FIG. 2

Related Art

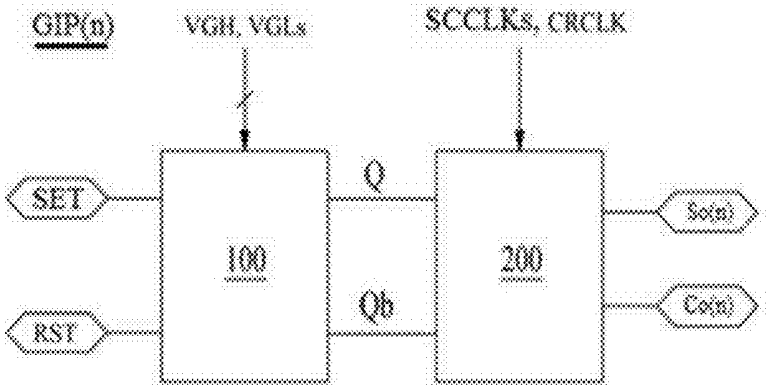


FIG. 3

Related Art

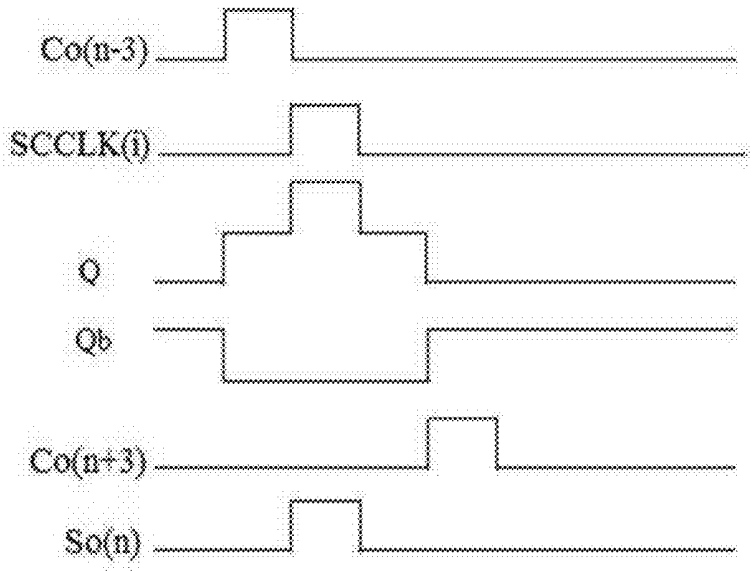
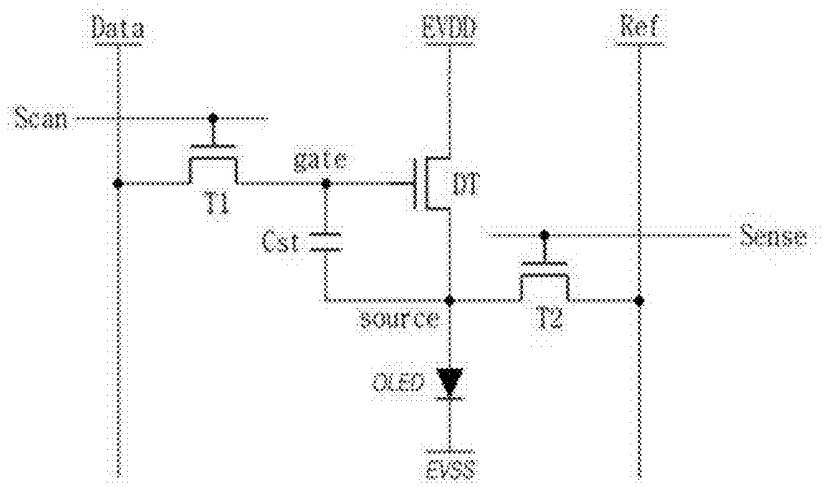


FIG. 4



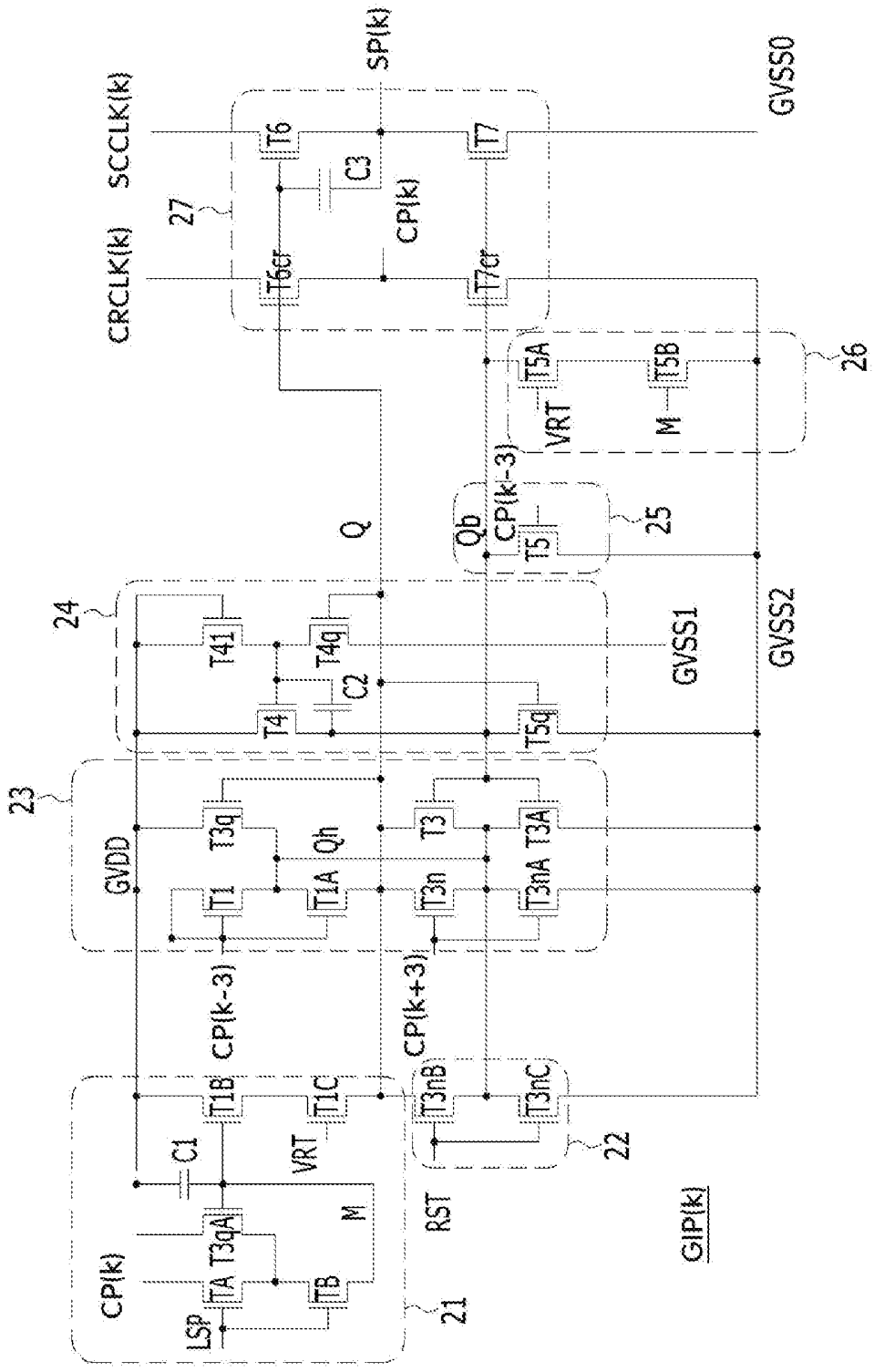

SP(k)
GVSS0
SCCLK(k)
CRCLK(k)
27
T6
C3
T7
CP(k)
T6cr
T7cr
26
T5A
T5B
VRT
M
CP(k-3)
Qb
T5
25
Q
24
T41
T4q
GVSS1
GVSS2
C2
T4
T5q
23
GVDD
T3q
Qh
T3
T3A
T1
T1A
T3n
T3nA
CP(k-3)
CP(k+3)
T1B
T1C
T3nB
T3nC
C1
VRT
22
RST
GIP(k)
CP(k)
T3qA
M
TA
TB
LSP
21

FIG. 6

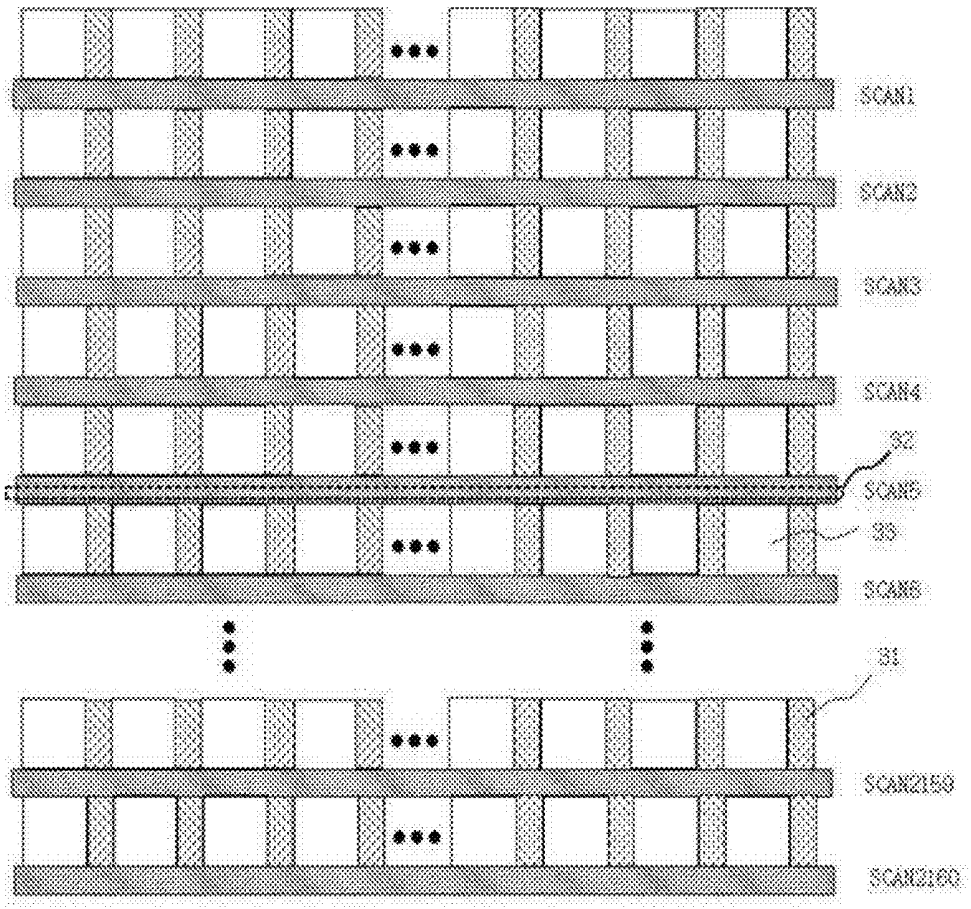

SCAN1
SCAN2
SCAN3
SCAN4
92
SCAN5
95
SCAN6
31
SCAN2159
SCAN2160

FIG. 7

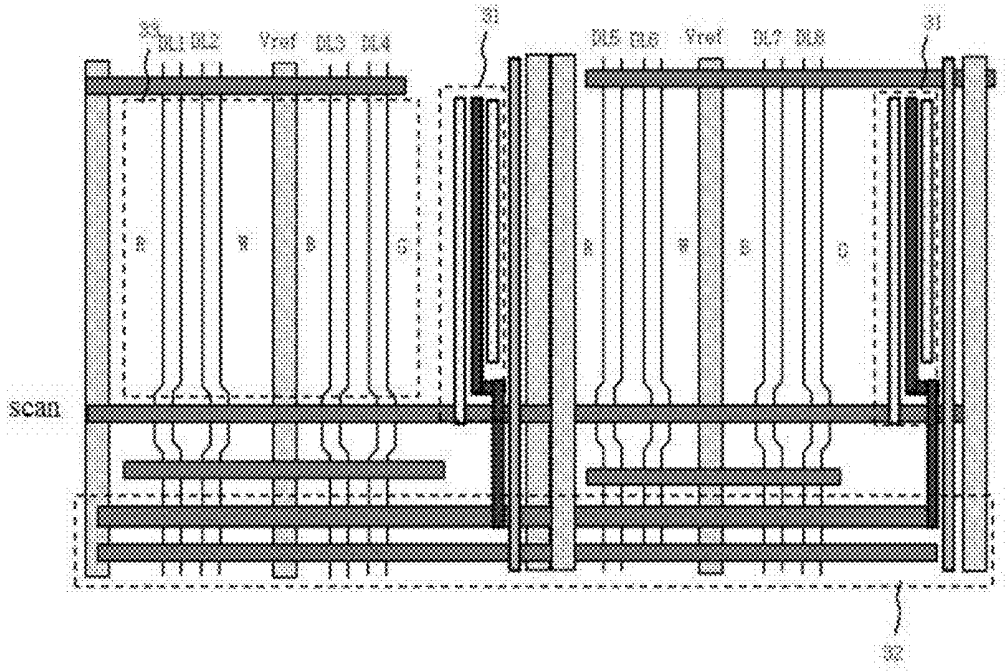

SL
BL1
BL2
Vref
BL3
BL4
31
BL5
BL6
Vref
BL7
BL8
31
R
W
B
G
R
W
B
G
scan
32

FIG. 8

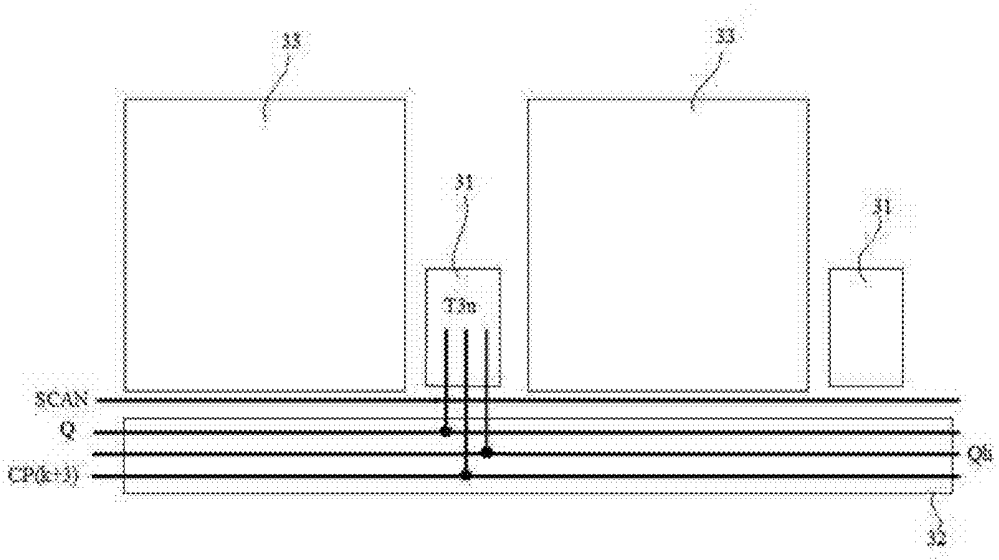
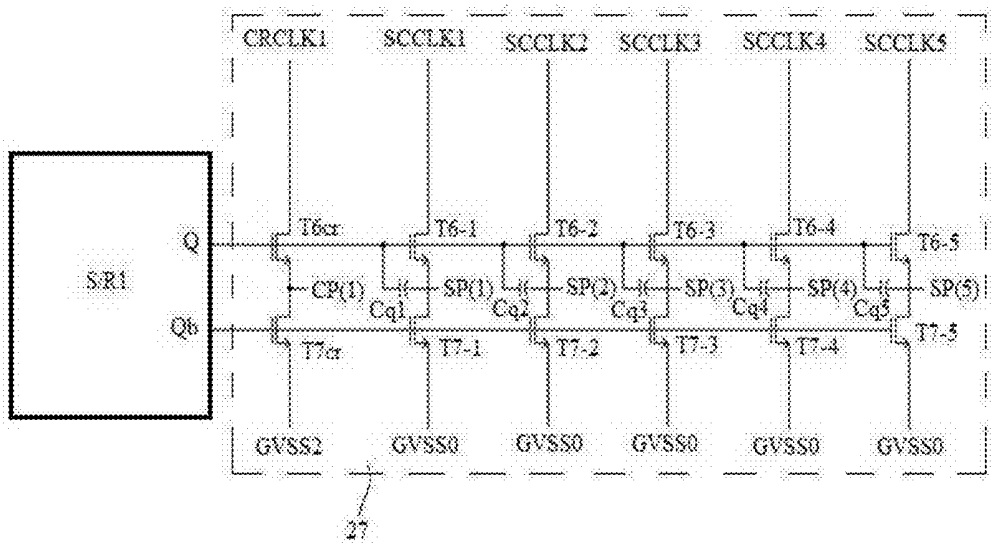

33
33
31
31
T3n
SCAN
Q
CP(k+1)
Qk
32

FIG. 9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SCCLK1
SCCLK2
SCCLK3
SCCLK4
SCCLK5
S.R1
Q
Qk
T6cr
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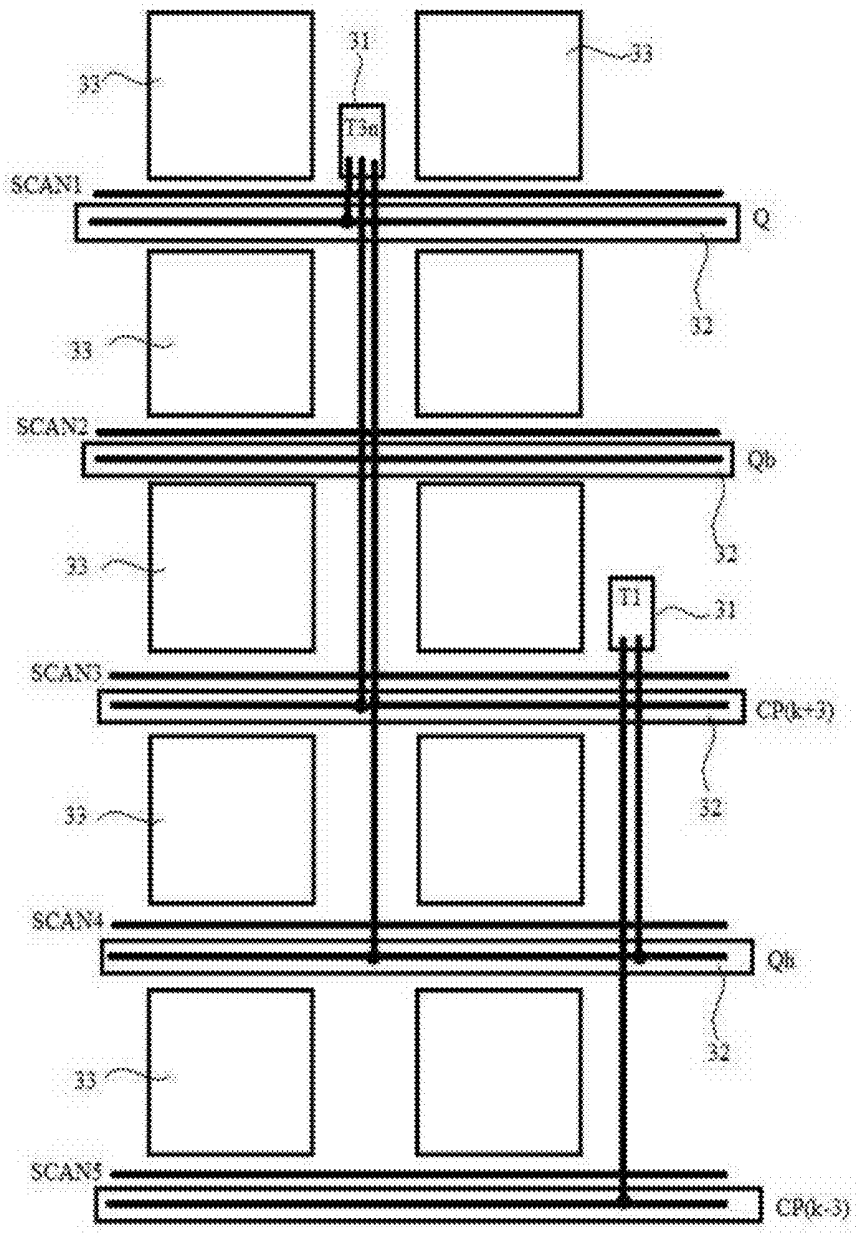
T6-2
T6-3
T6-4
T6-5
CP(1)
Cq1
SP(1)
Cq2
SP(2)
Cq3
SP(3)
Cq4
SP(4)
Cq5
SP(5)
T7cr
T7-1
T7-2
T7-3
T7-4
T7-5
GVSS2
GVSS0
GVSS0
GVSS0
GVSS0
GVSS0
27

FIG. 10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33
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T3n
SCAN1
Q
32
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SCAN2
Qb
32
33
T1
31
SCAN3
CP(k+3)
32
33
SCAN4
Qb
32
33
SCAN5
CP(k-3)

OLED DISPLAY PANEL AND OLED DISPLAY DEVICE COMPRISING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of Korean Patent Application No. 10-2017-0159650, filed on Nov. 27, 2017, which is hereby incorporated by reference in its entirety as if fully set forth herein.

BACKGROUND

Field of the Disclosure

[0002] The present disclosure relates to an OLED display panel and an OLED display device comprising the same, the OLED display panel having stages of a GIP driving circuit arranged in a pixel array and signal connection lines for constituting the GIP driving circuit.

Description of the Background

[0003] With the development of information society and various portable electronic devices such as mobile communication terminals and notebook computers, demand for flat panel display devices applicable to the electronic devices has increased.

[0004] A liquid crystal display (LCD) and an organic light-emitting diode (OLED) display device using an OLED are used as such flat panel display devices.

[0005] Such a flat panel display device is composed of a display panel including a plurality of gate lines and a plurality of data lines in order to display images, and a driving circuit for driving the display panel.

[0006] Among the aforementioned display devices, a display panel of the LCD includes a thin film transistor array substrate having a thin film transistor array formed on a glass substrate, a color filter array substrate having a color filter array formed on a glass substrate, and a liquid crystal layer interposed between the thin film transistor array substrate and the color filter array substrate.

[0007] The thin film transistor array substrate includes a plurality of gate lines GL extended in a first direction and a plurality of data lines DL extended in a second direction perpendicular to the first direction, and a sub-pixel region (pixel: P) is defined by each gate line and each data line. A thin film transistor and a pixel electrode are formed in the sub-pixel region P.

[0008] The display panel of the LCD displays an image by applying a voltage to electric field generation electrodes (a pixel electrode and a common electrode) to generate an electric field in the liquid crystal layer and adjusting the arrangement state of liquid crystal molecules of the liquid crystal layer through the electric field to control the polarization of incident light.

[0009] In addition, among the aforementioned display devices, a display panel of the OLED display device includes sub-pixels defined at the intersection of a plurality of gate lines and a plurality of data lines, and each sub-pixel includes an OLED composed of an anode, a cathode and an organic emission layer interposed between the anode and the cathode, and a pixel circuit for independently driving the OLED.

[0010] The pixel circuit can be configured in various manners and includes at least one switching TFT, a capacitor and a driving TFT.

[0011] The at least one switching TFT charges a data voltage in the capacitor in response to a scan pulse. The driving TFT controls the quantity of current supplied to the OLED in response to the data voltage charged in the capacitor to adjust the quantity of emitted light of the OLED.

[0012] Such a display panel for display devices is defined by an active area (AA) through which an image is display to a user and a non-active area (NA) that is a peripheral area of the active area AA.

[0013] In addition, the driving circuit for driving the display panel includes a gate driving circuit for sequentially supplying gate pulses (or scan pulses) to the plurality of gate lines (scan lines), a data driving circuit for supplying a data voltage to the plurality of data lines, and a timing controller for supplying image data and various control signals to the gate driving circuit and the data driving circuit.

[0014] Although the gate driving circuit may be composed of at least one gate drive IC, the gate driving circuit may be simultaneously formed on the non-active area of the display panel in a process of forming the plurality of signal lines (gate lines and data lines) and sub-pixels of the display panel.

[0015] That is, a Gate-In-Panel (GIP) method of integrating the gate driving circuit into the display panel is applied.

[0016] The aforementioned gate driving circuit includes a larger number of stages than the number of gate lines in order to sequentially supply scan pulses to the gate lines. Each stage is composed of an oxide semiconductor TFT in order to improve driving characteristics.

[0017] That is, the gate driving circuit includes a plurality of cascaded stages. In addition, each stage includes an output unit which is connected to each gate line (scan line). Each stage receives a clock signal, a gate start signal, a gate high voltage and a gate low voltage from the timing controller and generates a carry pulse and a scan pulse.

[0018] FIG. **1** is a block diagram showing driving circuits of the conventional OLED display device and a relationship between driving circuits.

[0019] Referring to FIG. **1**, an OLED display device **100** includes an OLED display panel PNL and driving circuits for applying input image data to a pixel array **110** of the OLED display panel PNL.

[0020] The OLED display panel PNL includes a plurality of gate lines **149** and a plurality of data lines **139** arranged in an intersecting manner, and the pixel array **110** in which sub-pixels defined by the plurality of gate lines **149** and the plurality of data lines **139** are arranged in a matrix form.

[0021] Each sub-pixel includes an OLED composed of an anode, a cathode and an organic emission layer interposed between the anode and the cathode, and a pixel circuit for independently driving the OLED.

[0022] The pixel circuit may be configured in various manners and includes at least one switching TFT, a capacitor and a driving TFT.

[0023] The driving circuits for driving the OLED display panel PNL include a data driving circuit **130** which is formed in a non-active area and supplies a data voltage to the plurality of data lines **139**, a GIP driving circuit **140** which is formed in the non-active area and sequentially supplies a

gate (scan) signal synchronized with the data voltage to the plurality of gate lines **149**, and a timing controller (TCON) **120**.

[0024] The timing controller **120** is disposed on a printed circuit board (PCB), aligns input image data received from an external host system and supplies the aligned input image data to the data driving circuit **130**. In addition, the timing controller **120** receives timing signals, such as a vertical synchronization signal, a horizontal synchronization signal, a data enable signal and a dot clock signal, synchronized with the input image, from the external host system and generates control signals (a data driver control signal DDC and a gate driver control signal GDC) for controlling operation timing of the data driving circuit **130** and the GIP driving circuit **140**.

[0025] The data driving circuit **130** receives the input image data and the data driver control signal DDC from the timing controller **120** and converts the input image data into a gamma compensated voltage to generate a data voltage and outputs the data voltage to the plurality of data lines **139**.

[0026] The data driving circuit **130** includes a plurality of source drive integrated circuits (ICs), each of which is configured in the form of a chip on film (COF) and each of which is connected between a pad part of the printed circuit board on which the timing controller **120** is mounted and a pad part of the display panel PNL.

[0027] The GIP driving circuit **140** may be disposed at one edge or both edges of the display panel PNL depending on driving method. The gate driving circuit **140** shown in FIG. **1** is an interlaced GIP driving circuit and includes a first GIP driving circuit **140**L disposed on the left side of the display panel PNL and a second GIP driving circuit **140**R disposed on the right side of the display panel PNL.

[0028] While the GIP driving circuit **140** may be composed of at least one gate drive IC, the GIP driving circuit **140** may be simultaneously formed with the plurality of signal lines (gate lines and data lines) and sub-pixels which constitute the pixel array **110** of the OLED display panel PNL in the non-active area of the display panel through a process of forming the signal lines and sub-pixels.

[0029] That is, the Gate-In-Panel (GIP) method of integrating the gate driving circuit into the display panel is applied.

[0030] The GIP driving circuit **140** sequentially supplies a gate (scan) signal to the gate lines **149** in response to the control signal GDC transmitted from the timing controller **120**.

[0031] The aforementioned GIP driving circuit **140** includes a larger number of stages ("GIP" hereinafter) than the number of gate lines in order to sequentially supply a scan pulse to the gate lines and uses oxide semiconductor thin film transistors in order to improve driving characteristics.

[0032] That is, the GIP driving circuit **140** includes a plurality of cascaded stages GIP. In addition, each stage GIP includes an output unit which is connected to each gate line. Each stage GIP receives a clock signal, a gate start signal, a gate high voltage and a gate low voltage supplied from the timing controller and generates a carry pulse and a scan pulse.

[0033] FIG. **2** is a block diagram of a normal n-th stage GIP.

[0034] As shown in FIG. **2**, each stage GIP includes a node controller **100** which is set by a start pulse or a carry pulse SET output from the previous stage GIP and reset by a carry pulse RST output from the next stage GIP to control voltages of first and second nodes Q and Qb, and an output unit **200** which receives one of a plurality of clock signals SCCLKs for scan pulse output and one of a plurality of clock signals CRCLKs for carry pulse output and outputs a scan pulse So(n) and a carry pulse Co(n) in response to voltage levels of the first and second nodes Q and Qb.

[0035] In the case of a stage GIP driven by a 6-phase clock signal, the node controller **100** is set by a carry pulse Co(n−3) output from the third previous stage GIP and is reset by a carry pulse Co(n+3) output from the third next stage GIP to control the voltages of the first and second nodes Q and Qb.

[0036] Although not shown in the figure, the output unit **200** of the stage GIP includes a carry pulse output unit and a scan pulse output unit.

[0037] The carry pulse output unit includes a first pull-up transistor and a first pull-down transistor which are serially connected between a carry pulse output clock signal terminal to which one of the plurality of clock signals for carry pulse output is applied and a first gate low voltage terminal VGL**1**.

[0038] The first pull-up transistor is turned on/off in response to the voltage level of the first node Q and the first pull-down transistor is turned on/off in response to the voltage level of the second node Qb to output the input carry pulse output clock signal as a carry pulse Co(n).

[0039] The scan pulse output unit includes a second pull-up transistor and a second pull-down transistor which are serially connected between a scan pulse output clock signal terminal to which one of the plurality of clock signals for scan pulse output is applied and a second gate low voltage terminal VGL**2**, and a bootstrap capacitor connected between the gate electrode and the source electrode of the second pull-up transistor.

[0040] The second pull-up transistor is turned on/off in response to the voltage level of the first node Q and the second pull-down transistor is turned on/off in response to the voltage level of the second node Qb to output the input scan pulse output clock signal as a scan pulse So(n).

[0041] FIG. **3** is a waveform diagram showing the operation of the n-th stage GIP shown in FIG. **2**.

[0042] FIG. **3** shows that the node controller **100** is set by the carry pulse Co(n−3) output from the third previous stage GIP and reset by the carry pulse Co(n+3) output from the third next stage GIP to control the voltages of the first and second nodes Q and Qb.

[0043] The n-th stage GIP(n) is set by the carry pulse Co(n−3) output from the third previous stage GIP to charge the first node Q with a gate high voltage VGH and to discharge the second node Qb to a gate low voltage VGL. Accordingly, the first pull-up transistor of the carry pulse output unit and the second pull-up transistor of the scan pulse output unit are turned on and the first pull-down transistor of the carry pulse output unit and the second pull-down transistor of the scan pulse output unit are turned off.

[0044] In addition, clock signals CRCLK and SCCLK having the same phase are applied to the drain electrode of the first pull-up transistor of the carry pulse output unit and the drain electrode of the second pull-up transistor of the scan pulse output unit.

[0045] When the clock signals CRCLK and SCCLK corresponding to a high level are applied to the drain electrode of the first pull-up transistor and the drain electrode of the second pull-up transistor, the voltage of the floated first node Q is bootstrapped by the bootstrap capacitor to increase by 2 VGH.

[0046] In a state in which the first node Q is bootstrapped in this manner, the carry pulse output unit and the scan pulse output unit respectively output the input clock signals CRCLK and SCCLK as a carry pulse Co(n) and a scan pulse So(n).

[0047] In addition, the stage is reset by the carry pulse Co(n+3) output from the third next stage GIP and thus the first node Q becomes a low state and the second node Qb becomes a high state. Accordingly, the first pull-up transistor of the carry pulse output unit and the second pull-up transistor of the scan pulse output unit are turned off and the first pull-down transistor of the carry pulse output unit and the second pull-down transistor of the scan pulse output unit are turned on to output the gate low voltage VGL as the carry pulse Co(n) and the scan pulse So(n).

[0048] However, the GIP driving circuit is integrated in the non-active area of the display panel in the conventional OLED display panel, as described above, and thus it is difficult to design a display device with a narrow bezel.

SUMMARY

[0049] Accordingly, the present disclosure devised to solve the aforementioned problem is to provide an OLED display panel and an OLED display device for disposing the signal connection lines for a GIP driving circuit in an active area and for minimizing the number of the signal connection lines in order to minimize the size of a bezel.

[0050] An OLED display panel according to the present disclosure to accomplish the object includes: an active area including data lines, scan lines intersecting the data lines, and sub-pixels arranged at each intersection; and a stage of a GIP driving circuit distributed and arranged in a plurality of unit pixel regions driven by m (m being a natural number) scan lines in the active area, to supply scan pulses to the corresponding scan lines, wherein the active area further includes m GIP internal connection lines parts respectively adjacent to the m scan lines, and a plurality of internal connection lines for connecting elements constituting each stage may be distributed and arranged in the m GIP internal connection line parts.

[0051] Here, each stage includes: a logic unit for controlling voltage levels of a first node and a second node using a carry pulse of the previous stage and a carry pulse of the next stage; a carry pulse output unit for outputting an input carry pulse output clock signal as a carry pulse in response to the voltage levels of the first node and the second node; and m scan pulse output units for respectively outputting input scan pulse output clock signals to the m scan lines as scan pulses in response to the voltage levels of the first node and the second node.

[0052] An OLED display device according to the present disclosure to accomplish the object includes an OLED display panel, which includes: an active area including data lines, scan lines intersecting the data lines, and sub-pixels arranged at each intersection; and a stage of a GIP driving circuit distributed and arranged in a plurality of unit pixel regions driven by m (m being a natural number) scan lines in the active area, to supply scan pulses to the corresponding scan lines, wherein the active area further includes m GIP internal connection lines parts respectively adjacent to the m scan lines, and a plurality of internal connection lines for connecting elements constituting each stage may be distributed and arranged in the m GIP internal connection line parts.

[0053] Each of the unit pixel regions may include at least three sub-pixels, a GIP part in which one element constituting each stage of the GIP driving circuit is arranged, and the plurality of internal connection lines arranged in the m GIP internal connection line parts may be extended to the GIP part and electrically connected to the elements constituting each stage.

[0054] The OLED display panel having the aforementioned characteristics according to the present disclosure has the following advantages.

[0055] That is, an OLED display panel according to a first aspect of the present disclosure can arrange the internal connection lines in the GIP internal connection line parts in the active area.

[0056] Moreover, an OLED display panel according to a second aspect of the present disclosure can reduce the number of internal connection lines arranged in GIP internal connection line parts because an output buffer includes a plurality of scan pulse output units, GIP elements are distributed and arranged in unit pixels driven by as many scan lines as the number of scan pulse output units, and internal connection lines (the node Q, the node Qb, the node Qh, connection lines connected to the carry pulse output terminal of the previous stage and the carry pulse output terminal of the next stage) are distributed and arranged in GIP internal connection line parts adjacent to the scan lines.

[0057] Accordingly, the size of a bezel of the OLED display panel according to the first aspect of the present disclosure can be reduced.

[0058] Accordingly, the aperture ratio of the OLED display panel according to the second aspect of the present disclosure can increase and the area occupied by the GIP internal connection line parts can be reduced, and thus a high-definition display panel can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0059] FIG. **1** is a block diagram showing driving circuits of the conventional OLED display device and a relationship between driving circuits.

[0060] FIG. **2** is a block diagram of a normal n-th stage GIP.

[0061] FIG. **3** is a waveform diagram showing the operation of the n-th stage GIP shown in FIG. **2**.

[0062] FIG. **4** is a circuit diagram of a sub-pixel in an OLED display panel according to an aspect of the present disclosure.

[0063] FIG. **5** is a circuit diagram of a k-th stage of a GIP driving circuit according to an aspect of the present disclosure.

[0064] FIG. **6** is a diagram showing a configuration of an active area of an OLED display panel according to a first aspect of the present disclosure.

[0065] FIG. **7** is a diagram showing a detailed configuration of two neighboring unit pixel regions arranged in the active area of the OLED display panel of FIG. **6**.

[0066] FIG. **8** is a diagram for describing internal connection lines arranged in a GIP internal connection line part according to the first aspect of the present disclosure.

[0067] FIG. **9** is a block diagram of an n-th stage GIP according to a second aspect of the present disclosure.

[0068] FIG. **10** is a diagram for describing internal connection lines arranged in a GIP internal connection line part according to the second aspect of the present disclosure.

DETAILED DESCRIPTION

[0069] The applicant applied the technology of distributing and arranging GIP driving circuits in an active area of a display panel in order to minimize the size of a bezel of the display panel (Korean Patent Application No. 10-2017-0125355 (Filing date: Oct. 27, 2017)).

[0070] The disclosure of Korean Patent Application (10-2017-0125355) will be briefly described as follows.

[0071] FIG. **4** is a circuit diagram of a sub-pixel in an OLED display panel according to the present disclosure and FIG. **5** is a circuit diagram of a k-th stage of a GIP driving circuit according to an aspect of the present disclosure.

[0072] That is, FIG. **4** corresponds to FIG. 4 of the Korean Patent Application (10-2017-0125355) and FIG. **5** corresponds to FIG. 5 of the Korean Patent Application (10-2017-0125355).

[0073] As shown in FIG. **4**, each sub-pixel of the OLED display panel according to an aspect of the present disclosure includes an OLED and a pixel circuit for driving the OLED.

[0074] The pixel circuit includes first and second switching TFTs T**1** and T**2**, a storage capacitor Cst and a driving TFT DT.

[0075] The first switching TFT T**1** charges a data voltage DATA in the storage capacitor Cst in response to a scan pulse signal. The driving TFT DT controls the quantity of current supplied to the OLED according to the data voltage charged in the storage capacitor Cst to adjust the quantity of emitted light of the OLED. The second switching TFT T**2** senses the threshold voltage and mobility of the driving TFT DT in response to a sense signal.

[0076] The OLED may be composed of a first electrode (e.g., anode or cathode), an organic emission layer and a second electrode (e.g., cathode or anode).

[0077] The storage capacitor Cst is electrically connected between the gate and the source of the driving TFT DT to maintain a data voltage corresponding to an image signal voltage or a voltage corresponding thereto for one frame period.

[0078] Although FIG. **4** shows a 3T1C sub-pixel configuration composed of three TFTs T**1**, T**2** and DT and one storage capacitor Cst, the present disclosure is not limited thereto and each sub-pixel of the OLED display panel according to the present disclosure may have a 4T1C, 4T2C, 5T1C or 5T2C sub-pixel configuration.

[0079] Meanwhile, as shown in FIG. **5**, the circuit of the k-th stage of the GIP driving circuit according to an aspect of the present disclosure includes: blank time first and second node controllers **21** and **26**, which include transistors TA, TB, T**3***q*A, T**1**B, T**1**C, T**5**A and T**5**B and a capacitor C**1**, selectively store a set signal CP(k) according to a line select pulse (LSP), charge a first node Q of the corresponding stage with a first constant voltage GVDD and discharge a second node Qb to a second constant voltage GVSS**2** according to a vertical real-time (VRT) signal in a blank time; driving time first to third node controllers **23** and **25**, which include transistors T**1**, T**1**A, T**3***n*, T**3***n*A, T**3***q*, T**3**, T**3**A and T**5**, charge the first node Q of the corresponding stage with the voltage of a carry pulse CP(k−3) of the third previous stage according to the carry pulse CP(k−3), discharge the first node Q and a third node Qh to a second constant voltage GVSS**2** according to a carry pulse CP(k+3) of the third next stage, and charge the third node Qh with the first constant voltage GVDD according to the voltage of the first node in a driving time; an inverter **24**, which includes transistors T**4**, T**4***l*, T**4***q* and T**5***q* and a capacitor C**2**, inverts the voltage of the first node Q and applies the inverted voltage to the second node Qb; an output buffer **27**, which includes pull-up transistors T**6***cr* and T**6**, pull-down transistors T**7***cr* and T**7** and a bootstrapping capacitor C**3**, receives one clock signal CRCLK(k) among a plurality of clock signals for carry pulse output and one clock signal SCCLK(k) among a plurality of clock signals for scan pulse output, and outputs a carry pulse CP(k) and a scan pulse SP(k) according to the voltages of the first node Q and the second node Qb; and a reset unit **22** which includes transistors T**3***n*B and T**3***n*C and discharges the first node Q to the second constant voltage GVSS**2** according to a reset signal RST output from the timing controller in the blank time.

[0080] The transistors TB, TA and T**3***q* in the blank time first and second node controllers **21** and **26** are turned on to store the set signal CP(k) in the capacitor C**1** when the LSP is at a high level.

[0081] In addition, the transistors T**1**C and T**5**B are turned on to charge the first node Q with the first constant voltage GVDD and to discharge the second node Qb to the second constant voltage GVSS**2** when the VRT signal is at a high level in the blank time.

[0082] The transistors T**1**, T**1**A and T**5** in the driving time first to third node controllers **23** and **25** are turned on to charge the first node Q with the carry pulse CP(k−3) of the third previous stage and to discharge the second node Qb to the second constant voltage GVSS**2** when the carry pulse CP(k−3) of the third previous stage is at a high level in the driving time. When the first node Q is charged and the second node Qb is discharged in this manner, the transistor T**3***q* is turned on to charge the third node Qh with the first constant voltage GVDD.

[0083] When the carry pulse CP(k+3) of the third next stage is at a high level, the transistors T**3***n* and T**3***n*A are turned on to discharge the first node Q and the third node Qh to the second constant voltage GVSS**2**.

[0084] The inverter **24** inverts the voltage of the first node Q and applies the inverted voltage to the second node Qb.

[0085] In the output buffer **27**, the pull-up transistor T**6***cr* is turned on and the pull-down transistor T**7***cr* is turned off to output one clock signal CRCLK(k) among the plurality of clock signals for carry pulse output as a carry pulse CP(k) when the first node Q is at a high level and the second node Qb is at a low level. Further, the pull-up transistor T**6** is turned on and the pull-down transistor T**7** is turned off to output one clock signal SCCLK(k) among the plurality of clock signals for scan pulse output as a scan pulse SP(k) when the first node Q is at a high level and the second node Qb is at a low level.

[0086] Here, when the clock signal SCCLK(k) for scan pulse output is applied at a high level, the bootstrapping capacitor C**3** of the output buffer **27** bootstraps (couples) the first node Q and thus the first node Q has a higher potential.

[0087] In this manner, the output buffer **27** outputs the clock signal CRCLK(k) for carry pulse output and the clock signal SCCLK(k) for scan pulse output, which are input

thereto, as a carry pulse CL(k) and a scan pulse SP(k) in a state in which the first node Q is bootstrapped, and thus output loss can be prevented.

[0088] In the reset unit **22**, the transistors T3*n*B and T3*n*C are turned on to discharge the first node Q to the second constant voltage GVSS**2** when the reset signal RST output from the timing controller is at a high level in the blank time.

[0089] Although FIG. **5** shows a stage of the GIP driving circuit driven with 6 phases, the present disclosure is not limited thereto and stages of the GIP driving circuit can be configured in various manners.

[0090] As shown in FIG. **5**, each stage of the GIP driving circuit includes 25 transistors and 3 capacitors.

[0091] Accordingly, when an element (transistor or capacitor) constituting the stage of the GIP driving circuit is distributed and arranged in a unit pixel region, the circuit of a stage for driving a gate line (scan line) can be arranged.

[0092] FIG. **6** is a diagram showing a configuration of the active area of the OLED display panel according to a first aspect of the present disclosure and FIG. **7** is a diagram showing a detailed configuration of two neighboring unit pixels arranged in the active area of the OLED display panel shown in FIG. **6**.

[0093] That is, FIG. **6** corresponds to FIG. 6 of the Korean Patent Application (10-2017-0125355) and FIG. **7** corresponds to FIG. 7 of the Korean Patent Application (10-2017-0125355).

[0094] As shown in FIGS. **6** and **7**, in arrangement of the GIP driving circuit in the active area of the OLED display panel, a unit pixel region of the active area is divided into at least three sub-pixels R, G, B and W, a GIP part **31** and a GIP internal interconnection line part **32**.

[0095] The at least three sub-pixels (R, G, B and W) **33** are configured in such a manner that a plurality of data lines DL**1** to DL**8**, a plurality of reference voltage lines Vref and first and second constant voltage lines EVDD and EVSS are arranged in the vertical direction and a plurality of gate lines (scan lines) SCAN are arranged in the horizontal direction.

[0096] The GIP part **31** corresponds to an element (transistor or capacitor) constituting a stage of the GIP driving circuit. That is, the element (transistor or capacitor) constituting the stage of the GIP driving circuit is distributed and arranged in a unit pixel region composed of red, green, blue and white sub-pixels R, G, B and W.

[0097] That is, at least one stage ST of the GIP driving circuit for driving a gate line (scan line) is distributed and arranged in a plurality of unit pixel regions driven by a gate line (scan line).

[0098] The GIP internal interconnection line part **32** is an area in which connection lines (a node Q, a node QB, a node Qh, a carry pulse output terminal of the previous stage, a carry pulse output terminal of the next stage, etc.) for connecting elements in a stage of the GIP driving circuit are arranged.

[0099] As described above, as the GIP driving circuit is arranged in the active area, the plurality of data lines DL**1** to DL**8** and the reference voltage lines Vref for driving the sub-pixels R, G, B and W are arranged in the vertical direction, as shown in FIG. **7**.

[0100] In addition, since the GIP part **31** corresponds to an element (transistor or capacitor) constituting a stage of the GIP driving circuit, one of the signals LSP, VRT, GVDD, GVSS**0**, GVSS**1**, GVSS**2**, VST, CRCLK and SCCLK shown in FIG. **5** is applied to the GIP part **31**.

[0101] Furthermore, in the OLED display panel according to the first aspect of the present disclosure, the circuit of a stage for driving a gate line (scan line) is distributed and arranged in unit pixel regions driven by the gate line (scan line) and thus all connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) for connecting elements in the stage of the GIP driving circuit need to be arranged in the GIP internal connection line part **32** corresponding to the gate line (scan line).

[0102] FIG. **8** shows internal connection lines arranged in the GIP internal connection line part **32** according to the first aspect of the present disclosure.

[0103] In FIG. **5**, a signal line CP(k+3) to which a carry pulse output from the third next stage is applied is connected to the gate electrode of the transistor T3*n*, the node Q is connected to the source electrode of the transistor T3*n*, and the node Qh is connected to the drain electrode of the transistor T3*n*, for example.

[0104] Accordingly, when it is assumed that the transistor T3*n* shown in FIG. **5** is arranged in a GIP part **31**, at least the signal line CP(k+3), to which the carry pulse output from the third next stage is applied, the node Q and the node Qb need to be arranged in the GIP internal connection line part **32**.

[0105] In this manner, the circuit of a stage for driving a gate line (scan line) is distributed and arranged in unit pixel regions driven by the gate line (scan line) in the OLED display panel according to the first aspect of the present disclosure, and thus a maximum of four GIP internal connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) are arranged in the GIP internal connection line part **32** of each line. For example, a connection line between elements corresponds to a connection line between the gate electrode of the transistor T**4** and the drain electrode of the transistor T**4***l* in FIG. **5**.

[0106] Accordingly, the aperture ratio of the OLED display panel according to the first aspect of the present disclosure decreases and the area occupied by the GIP internal connection line parts **32** increases, and thus the OLED display panel is not suitable for high definition.

[0107] To solve this problem, in an OLED display panel and an OLED display device according to a second aspect of the present disclosure, the stages of the GIP driving circuit are arranged in the pixel array to increase the aperture ratio of the OLED display panel while providing a narrow bezel and to reduce the area occupied by the GIP internal connection line parts, realizing high definition.

[0108] FIG. **9** is a block diagram of the n-th stage GIP according to the second aspect of the present disclosure.

[0109] In the OLED display panel according to the second aspect of the present disclosure, the stages of the GIP driving circuit are arranged in the pixel array in such a manner that a stage including a plurality of scan pulse output units is configured for unit pixels driven by a plurality of scan lines.

[0110] That is, the circuit of the k-th stage of the GIP driving circuit according to an aspect of the present disclosure includes the blank time first and second node controllers **21** and **26**, the driving time first to third node controllers **23** and **25**, the inverter **24**, the output buffer **27** and the reset unit **22**, as described above with reference to FIG. **5**.

[0111] However, the OLED display panel according to the second aspect of the present disclosure has the stages of the GIP driving circuit, which are arranged in the pixel array, wherein the blank time first and second node controllers **21** and **26**, the driving time first to third node controllers **23** and **25**, the inverter **24** and the reset unit **22**, which are described above with reference to FIG. **5**, and the output buffer **27** including a carry pulse output unit and a plurality of scan pulse output units are arranged in unit pixels driven by a plurality of scan lines, as shown in FIG. **9**.

[0112] In FIG. **9**, the blank time first and second node controllers **21** and **26**, the driving time first to third node controllers **23** and **25**, the inverter **24** and the reset unit **22**, which are described above with reference to FIG. **5**, are represented by a logic unit S/R**1**.

[0113] The logic unit S/R**1** controls the voltage levels of the first node Q and the second node Qb using the line select signal LSP, the set signal CP(k), the vertical real-time signal VRT, the carry pulse CP(k−3) of the m-th previous stage, the carry pulse CP(k+3) of the m-th next stage and the reset signal RST, as described in FIG. **5**.

[0114] In addition, the output buffer **27** includes a carry pulse output unit and a plurality of scan pulse output units.

[0115] That is, the output buffer **27** includes: a carry pulse output unit composed of a pull-up transistor T**6***cr* and a pull-down transistor T**7***cr*, and configured in such a manner that the pull-up transistor T**6***cr* is turned on and the pull-down transistor T**7***cr* is turned off to output a clock signal CRCLK**1** among the plurality of carry pulse output clock signals as a carry pulse CP(**1**) when the first node Q is at a high level and the second node Qb is at a low level; a first scan pulse output unit composed of a first pull-up transistor T**6-1**, a first pull-down transistor T**7-1** and a first bootstrapping capacitor Cq**1**, and configured in such a manner that the first pull-up transistor T**6-1** is turned on and the first pull-down transistor T**7-1** is turned off to output a clock signal SCCLK(**1**) among the plurality of scan pulse output clock signals as a scan pulse SP(**1**) when the first node Q is at a high level and the second node Qb is at a low level; a second scan pulse output unit composed of a second pull-up transistor T**6-2**, a second pull-down transistor T**7-2** and a second bootstrapping capacitor Cq**2**, and configured in such a manner that the second pull-up transistor T**6-2** is turned on and the second pull-down transistor T**7-2** is turned off to output a clock signal SCCLK(**2**) among the plurality of scan pulse output clock signals as a scan pulse SP(**2**) when the first node Q is a high level and the second node Qb is a low level; a third scan pulse output unit composed of a third pull-up transistor T**6-3**, a third pull-down transistor T**7-3** and a third bootstrapping capacitor Cq**3**, and configured in such a manner that the third pull-up transistor T**6-3** is turned on and the third pull-down transistor T**7-3** is turned off to output a clock signal SCCLK(**3**) among the plurality of scan pulse output clock signals as a scan pulse SP(**3**) when the first node Q is at a high level and the second node Qb is at a low level; a fourth scan pulse output unit composed of a fourth pull-up transistor T**6-4**, a fourth pull-down transistor T**7-4** and a fourth bootstrapping capacitor Cq**4**, and configured in such a manner that the fourth pull-up transistor T**6-4** is turned on and the fourth pull-down transistor T**7-4** is turned off to output a clock signal SCCLK(**4**) among the plurality of scan pulse output clock signals as a scan pulse SP(**4**) when the first node Q is at a high level and the second node Qb is at a low level; and a fifth scan pulse output unit composed of a fifth pull-up transistor T**6-5**, a fifth pull-down transistor T**7-5** and a fifth bootstrapping capacitor Cq**5**, and configured in such a manner that the fifth pull-up transistor T**6-5** is turned on and the fifth pull-down transistor T**7-5** is turned off to output a clock signal SCCLK(**5**) among the plurality of scan pulse output clock signals as a scan pulse SP(**5**) when the first node Q is at a high level and the second node Qb is at a low level.

[0116] When the output buffer **27** includes one carry pulse output unit and five scan pulse output units, as shown in FIG. **9**, elements constituting the stage having the logic unit S/R**1** and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by five scan lines in the OLED display panel according to the second aspect of the present disclosure.

[0117] Although the output buffer **27** includes one carry pulse output unit and five scan pulse output units in FIG. **9**, the present disclosure is not limited thereto and the output buffer **27** may include one carry pulse output unit and at least two scan pulse output units.

[0118] If the output buffer **27** includes one carry pulse output unit and two scan pulse output units, the elements constituting the stage having the logic unit S/R**1** and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by two scan lines in the OLED display panel according to the second aspect of the present disclosure.

[0119] Further, when the output buffer **27** includes one carry pulse output unit and three scan pulse output units, the elements constituting the stage having the logic unit S/R**1** and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by three scan lines in the OLED display panel according to the second aspect of the present disclosure.

[0120] That is, in the OLED display panel according to the second aspect of the present disclosure, the elements constituting the stage having the logic unit S/R**1** and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by as many scan lines as the number of scan pulse output units.

[0121] Line arrangement of the GIP internal connection line parts when the stage having the aforementioned configuration is arranged in the corresponding area will be described below.

[0122] FIG. **10** is a diagram for describing internal connection lines arranged in the GIP internal connection line parts according to the second aspect of the present disclosure.

[0123] FIG. **10** illustrates internal connection lines when the output buffer **27** includes one carry pulse output unit and five scan pulse output units as shown in FIG. **9**.

[0124] That is, the elements constituting the stage having the logic unit S/R**1** and the output buffer **27** shown in FIG. **9** are distributed and arranged in arbitrary unit pixels among the unit pixels driven by the first to fifth scan lines SCAN**1** to SCAN**5**.

[0125] In addition, one of the internal connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) is arranged in each GIP internal connection line part **32** adjacent to each scan line SCAN**1** to SCAN**5**.

[0126] That is, the node Q is arranged in the GIP internal connection line part **32** adjacent to the first scan line

SCAN1, the node Qb is arranged in the GIP internal connection line part **32** adjacent to the second scan line SCAN2, the connection line CP(k+3) connected to the carry pulse output terminal of the next stage is arranged in the GIP internal connection line part **32** adjacent to the third scan line SCAN3, the node Qb is arranged in the GIP internal connection line part **32** adjacent to the fourth scan line SCAN4, and the connection line CP(k−3) connected to the carry pulse output terminal of the previous stage is arranged in the GIP internal connection line part **32** adjacent to the fifth scan line SCAN5.

[0127] In addition, the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9** are distributed and arranged in arbitrary unit pixels among the unit pixels driven by the first to fifth scan lines SCAN1 to SCAN5, as described above.

[0128] For example, the signal line CP(k+3) to which the carry pulse output from the third next stage is applied is connected to the gate electrode of the transistor T3*n* (refer to FIG. **5**) among the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9**, the node Q is connected to the source electrode of the transistor T3*n*, and the node Qh is connected to the drain electrode of the transistor T3*n*.

[0129] Accordingly, if the transistor T3*n* shown in FIG. **5** is arranged in the GIP part **31**, the node Q arranged in the GIP internal connection line part **32** adjacent to the first scan line SCAN1, the connection line CP(k+3) connected to the carry pulse output terminal of the next stage, which is arranged in the GIP internal connection line part **32** adjacent to the third scan line SCAN3, and the node Qh arranged in the GIP internal connection line part **32** adjacent to the fourth scan line SCAN4 are connected to the transistor T3*n*, as shown in FIG. **10**.

[0130] In addition, the signal line CP(k−3) to which the carry pulse output from the third previous stage is applied is connected to the gate electrode and the source electrode of the transistor T1 (refer to FIG. **5**) among the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9**, and the node Qh is connected to the source electrode of the transistor T1.

[0131] Accordingly, if the transistor T1 shown in FIG. **5** is arranged in the GIP part **31**, the node Qh arranged in the GIP internal connection line part **32** adjacent to the fourth scan line SCAN4 and the connection line CP(k−3) connected to the carry pulse output terminal of the previous stage, which is arranged in the GIP internal connection line part **32** adjacent to the fifth scan line SCAN53, are connected to the transistor T1, as shown in FIG. **10**.

[0132] Since the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9** are distributed and arranged in arbitrary unit pixels among the unit pixels driven by the first to fifth scan lines SCAN1 to SCAN5, as described above, GIP elements are not arranged in the GIP parts **31** of all unit pixels. Accordingly, signal lines extended to the GIP parts **31** and arranged in the GIP internal connection line parts **32** can be connected to the GIP elements.

[0133] Although FIG. **10** illustrates that the unit elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9** are distributed and arranged in arbitrary unit pixels among the unit pixels driven by the first to fifth scan lines SCAN1 to SCAN5, the present disclosure is not limited thereto and the unit elements constituting the stage may be distributed and arranged in arbitrary unit pixels among unit pixels driven by at least two scan lines.

[0134] If the output buffer **27** shown in FIG. **9** includes one carry pulse output unit and two scan pulse output units, the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by the first and second scan lines SCAN1 and SCAN2 in the OLED display panel according to the second aspect of the present disclosure. In addition, the internal connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) are distributed and arranged in two GIP internal connection line parts **32** adjacent to the first and second scan lines SCAN1 and SCAN2.

[0135] If the output buffer **27** shown in FIG. **9** includes one carry pulse output unit and three scan pulse output units, the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by the first to third scan lines SCAN1 to SCAN3 in the OLED display panel according to the second aspect of the present disclosure. In addition, the internal connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) are distributed and arranged in three GIP internal connection line parts **32** adjacent to the first to third scan lines SCAN1 to SCAN3.

[0136] That is, in the OLED display panel according to the second aspect of the present disclosure, the elements constituting the stage having the logic unit S/R1 and the output buffer **27** shown in FIG. **9** are distributed and arranged in unit pixels driven by as many scan lines as the number of scan pulse output units included in the output buffer **27**, and the internal connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) are distributed and arranged in GIP internal connection line parts **32** adjacent to the corresponding scan lines.

[0137] As described above, in the OLED display panel according to the second aspect of the present disclosure, the output buffer illustrated in FIG. **9** includes a plurality of scan pulse output units, GIP elements are distributed and arranged in unit pixels driven by as many scan lines as the number of scan pulse output units, and the internal connection lines (the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage, the carry pulse output terminal of the next stage, connection lines between elements, etc.) are distributed and arranged in GIP internal connection line parts **32** adjacent to the corresponding scan lines, and thus the number of internal connection lines arranged in the GIP internal connection lines parts **32** can be reduced.

[0138] Accordingly, the aperture ratio of the OLED display panel according to the second aspect of the present disclosure can increase and the area occupied by the GIP internal connection lines **32** can be reduced, and thus a high-definition display panel can be realized.

[0139] Those skilled in the art will appreciate that various modifications and variations can be made in the present disclosure without departing from the spirit or scope of the

present disclosure through the above description. Accordingly, the scope of the disclosure should be determined by the appended claims and their legal equivalents, not by the above description.

What is claimed is:

1. An OLED display panel, comprising:

a plurality of data lines and a plurality of scan lines intersecting the plurality of data lines, and a plurality of sub-pixels arranged at each intersection of the plurality of data lines and the plurality of scan lines at an active area;

a stage of a gate in panel (GIP) driving circuit arranged in a plurality of unit pixel regions driven by m (m being a natural number) scan lines in the active area and supplies scan pulses to the corresponding scan lines;

m GIP internal connection lines parts respectively adjacent to the m scan lines at the active area; and

a plurality of internal connection lines connecting elements constituting each stage arranged in the m GIP internal connection line parts.

2. The OLED display panel according to claim **1**, wherein each stage includes:

a logic unit controlling voltage levels of a first node and a second node using a carry pulse of a previous stage and a carry pulse of a next stage;

a carry pulse output unit outputting an input carry pulse output clock signal as a carry pulse in response to the voltage levels of the first node and the second node; and

m scan pulse output units respectively outputting clock signals to the m scan lines as scan pulses in response to the voltage levels of the first node and the second node.

3. The OLED display panel according to claim **1**, wherein each of the unit pixel regions includes at least three sub-pixels, a GIP part in which a unit element constituting each stage of the GIP driving circuit is arranged, and the plurality of internal connection lines arranged in the m GIP internal connection line parts extended to the GIP part and electrically connected to the unit element constituting each stage.

4. The OLED display panel according to claim **1**, wherein m GIP internal connection lines parts are included in areas respectively adjacent to the m scan lines, and a node Q, a node Qb, a node Qh, a carry pulse output terminal of the previous stage and a carry pulse output terminal of the next stage connecting the unit element constituting each stage is arranged in the m GIP internal connection line parts.

5. The OLED display panel according to claim **1**, wherein the m includes one of 2, 3 and 5.

6. An OLED display panel, comprising:

an active area including a plurality of data lines, a plurality of scan lines intersecting the plurality of data lines, and a plurality of sub-pixels arranged at each intersection; and

a stage of a GIP driving circuit, arranged in a plurality of unit pixel regions driven by one of two, three and five scan lines in the active area and supplying scan pulses to the corresponding scan lines,

wherein each stage includes:

a logic unit controlling voltage levels of a first node and a second node using a carry pulse of a previous stage and a carry pulse of a next stage;

a carry pulse output unit outputting a clock signal as a carry pulse in response to the voltage levels of the first node and the second node; and

one of two, three and five scan pulse output units matching a same number as the scan lines respectively outputting one of two, three and five clock signals to the one of two, three and five scan lines as scan pulses in response to the voltage levels of the first node and the second node.

7. The OLED display panel according to claim **6**, further comprising one of two, three and five GIP internal connection lines parts respectively adjacent to the one of two, three and five scan lines at the active area.

8. The OLED display panel according to claim **7**, further comprising a node Q, a node Qb, a node Qh, a carry pulse output terminal of a previous stage and a carry pulse output terminal of a next stage connecting a unit element constituting each stage arranged in each GIP internal connection line part.

9. The OLED display panel according to claim **8**, wherein each of the unit pixel regions includes at least three sub-pixels and a GIP part in which a unit element constituting each stage of the GIP driving circuit is arranged.

10. The OLED display panel according to claim **9**, wherein the node Q, the node Qb, the node Qh, the carry pulse output terminal of the previous stage and the carry pulse output terminal of the next stage, arranged in the one of two, three and five GIP internal connection line parts, are extended to the GIP part and electrically connected to the unit elements constituting each stage.

* * * * *

专利名称(译)	OLED显示面板和包括其的OLED显示装置		
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[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KIM KYUNG MIN HAN IN HYO SHIN HUN KI		
发明人	KIM, KYUNG-MIN HAN, IN-HYO SHIN, HUN-KI		
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外部链接	Espacenet USPTO		

摘要(译)

本发明涉及一种用于使边框的尺寸最小化的OLED显示面板，并且包括：有源区，包括数据线，与数据线交叉的扫描线，以及布置在每个交叉点处的子像素; GIP驱动电路的级分布在由有源区中的m（m为自然数）扫描线驱动的多个单位像素区中，以将扫描脉冲提供给相应的扫描线，其中，有源区进一步提供包括分别与m条扫描线相邻的m个GIP内部连接线部分，并且用于连接构成每个级的元件的多个内部连接线分布并布置在m个GIP内部连接线部分中。